REMARKS

Applicants appreciate the Examiner's thorough review of the present application that is evidenced in the Office Actions of December 15, 2004, April 7, 2005, September 22, 2005, February 9, 2006, June 5, 2006 and November 15, 2006. For the reasons discussed below, Applicants respectfully submit that each of these claims is patentable over the cited references.

I. The Claim Amendments

Applicants have cancelled non-elected Claims 13-21 and 33-37 such that only Claims 1-12, 38-40 and 45-46 remain pending in this case. Applicants have amended independent Claim 1 to correct a typographical error. Applicants have also made various amendments to dependent Claims 2-11, and have added new dependent Claims 47-54.

II. The Rejections Under 35 U.S.C. § 103

Claims 1-12, 38-40 and 45-46 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application No. 6,211,531 to Nakazato et al. ("Nakazato") in view of U.S. Patent No. 5,604,357 to Hori ("Hori"). (Office Action at 2-3). For the reasons discussed below, Applicants respectfully submit that the combination of Nakazato and Hori does not render any of the pending claims obvious.

A. The Rejection of Claim 1

Pending Claim 1 recites:

1. A semiconductor memory device, comprising:

a plurality of unit memory cells, wherein a unit memory cell comprises:

a first planar transistor in a semiconductor substrate;

a vertical transistor disposed on the first planar transistor; and

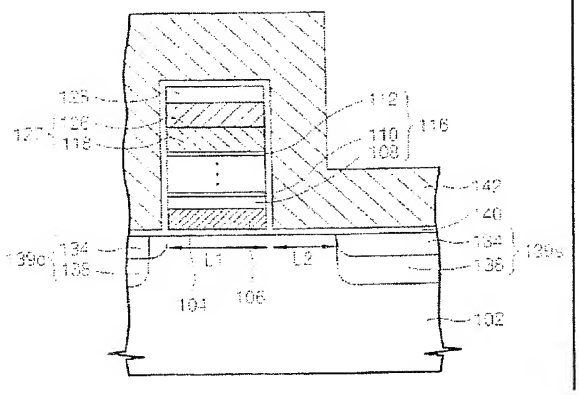
a second planar transistor in the semiconductor substrate, wherein the second planar transistor is electrically connected in series with the first planar transistor.

The Office Action states that Figure 16b of Nakazato discloses a planar transistor in a substrate with a vertical side gate tunneling transistor on the planar transistor, and that Figure

8 of Hori discloses "a MISFET for selection adjacent a tunnel device disposed on a planar transistor." (Office Action at 2). The Office Action further states that it "would have been obvious to include a MOSFET as taught by Figure 8 of Hori in the Nakazato device for the same purpose, i.e., to provide for selection circuitry as needed for a memory." (Office Action at 2). However, for the reasons discussed below, Applicants respectfully submit that the rejection of Claim 1 should be withdrawn.

Applicants respectfully submit there is no reason, suggestion or motivation for combining Nakazoto and Hori in the manner suggested in the pending rejections. Instead, Applicants submit that the combination of Nakazato and Hori suggested in the pending rejections reflects hindsight based on the teachings of the present invention.

In particular, as shown in Fig. 12A of the present application and as is expressly recited in pending Claim 4, in embodiments of the present invention the word line (142) is used as gate electrodes for both the second planar transistor and the vertical transistor.



In contrast, as shown in the following figures, Nakazato fails to disclose the second planar transistor of the present invention, and Hori fails to disclose the vertical transistor of the present invention. Additionally, it should also be noted that the **gate electrode 6 of Hori is used not only as a gate electrode for the Memory MISFET, but also as a gate electrode for the Selection MISFET**.

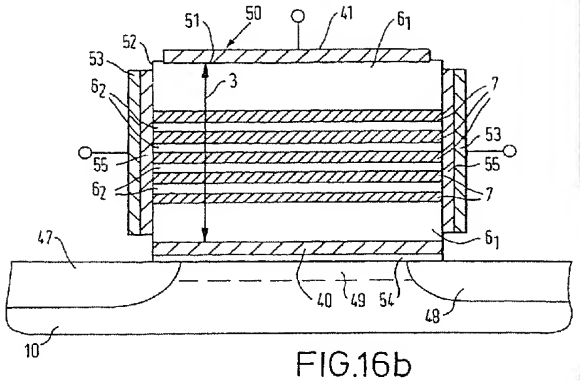
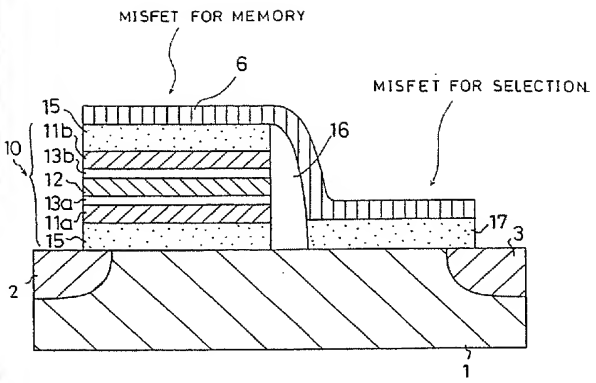


FIG.16b

U.S. Patent No. 6,211,531 (Nakazato et al.)



U.S. Patent No. 5,604,357 (Hori)

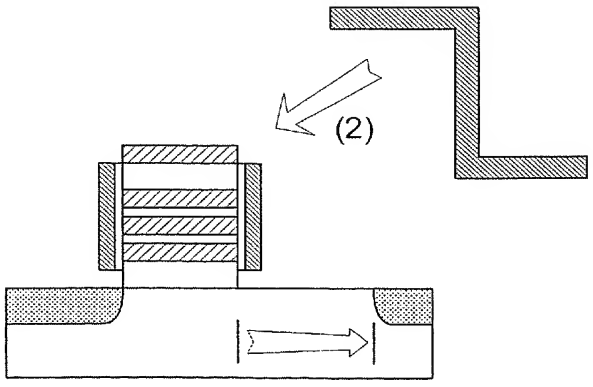
If a person of ordinary skill in the art were to combine Nakazato and Hori as suggested in the pending rejections, the following modifications would be required:

(1) The distance between the source/drain regions 47 and 48 of Nakazato would need to be widened to make room for the selection transistor of Hori; and

(2a) The gate electrode 6 of Hori would need to be substituted for the control electrode 41 of Nakazato; or

(2b) The gate electrode 6 of Hori would need to be substituted for the gate 53 of Nakazato.

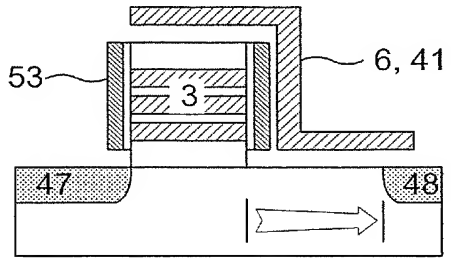
These modifications are illustrated graphically in the following drawing:



(1)

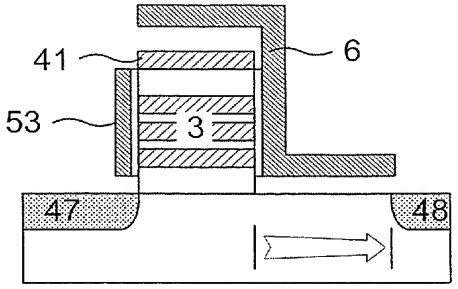
First, Applicants respectfully submit that there is **no suggestion for widening the distance between the source/drain regions 47 and 48 of Nakazato to make room for the selection transistor of Hori as shown in modification (1) in the above drawing**. Second, the

control electrode 41 and the gate 53 should be separated electrically with each other such that the device of Nakazato can be operated normally. Thus, in order to implement modification (2a) above, the control electrode 41 would be configured to be separate from the gate 53, as shown in the following figure.

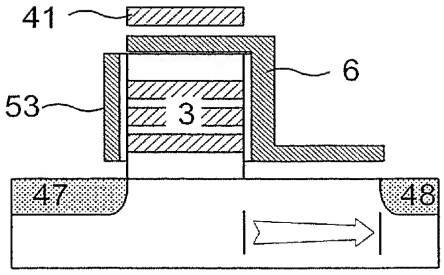


However, in this case, since the gate 53 is interposed between the gate electrode 6/41 and the multiple layer structure 3, it shields an electric field from gate electrode 6/41. As such, were Nakazato modified as suggested in modification (2a) above, the resulting device would not disclose or suggest using "the word line (142) . . . as gate electrodes of both the second planar transistor and the vertical transistor" as recited in pending Claim 4.

For modification (2b), the control electrode 41 should be interposed between the gate electrode 6 and the multiple layer structure 3 in order to provide the required separation between the control electrode 41 and the gate 53, as shown in the following figure.



In this case, since the control electrode 41 shields an electric field from the gate electrode 6, the gate electrode 6 cannot serve as a gate electrode for the memory MISFET. Therefore, this modification is incompatible with the requirement for Hori's device. Alternatively, modification (2b) might be configured as in the following figure.



However, since the control electrode 41 is separated from the multiple layer structure 3 by the gate electrode 6, this is incompatible with the requirement for Nakazato's device. Thus, for the above-stated reasons, Applicants respectfully submit that one of skill in the art would not have been motivated to combine Nakazato and Hori in the manner suggested in the pending rejections.

Applicants also respectfully submit that the pending rejections also fail to suggest a proper motivation for modifying Nakazato to include "selection MISFIT" of Figure 8 of Hori. In particular, Hori describes a MISFET device in which conductive carriers are moved between two storage regions 11a and 11b. In contrast, Nakazato describes memory devices in which charge is stored or released from a single "memory node 40." While Hori states that memory devices of the type described therein may be subject to a phenomena by which writing to one memory cell in the integrated circuit can have interference with an adjoining memory cell to change the storage state therein, their has been no showing that the memory cells of Nakazato are subject to such disturbances. (*See* Hori at Col. 17, lines 19-24). As such, no reason has been shown why one of ordinary skill in the art would include the selection MISFET of Hori in the device of Nakazato. Thus, for at least each of the above reasons, Applicants respectfully submit that one of ordinary skill in the art would not have been motivated to combine Nakazato and Hori in the manner suggested and, as such, respectfully request withdrawal of the rejection of Claim 1 for at least these reasons.

B. The Rejections of Claims 2-12 and 45-46

Dependent Claims 2-12 and 45-46 depend from Claim 1, and hence the rejections of these claims should be withdrawn for at least each of the reasons, discussed above, that the

rejection of Claim 1 should be withdrawn. Additionally, Applicants have rewritten dependent Claims 2-7 and 9-11 to further highlight the differences between embodiments of the present invention and the asserted combination of references, and Applicants submit that each of these claims, as revised herein, are independently patentable over the cited art. Claims 12 and 45-46 remain unamended, and Claim 8 is unamended except for a change in the dependency thereof. With respect to these claims, Applicants submit that at least Claims 8 and 12 are patentable over the cited art for at least the following additional reasons.

Claim 8 recites that "a portion of the first conductive region adjacent the channel is lightly doped as compared to a portion of the second conductive region adjacent the channel." The Office Action states that lightly doped drain regions are well known in the art, and hence obvious, to control high electric fields near the drain. Applicants respectfully submit, however, that this assertion fails to show that one of skill in the art would have been motivated to provide a first conductive region on one side of the channel that is lightly doped adjacent the channel while providing a second conductive region on the other side of the channel that is more heavily doped adjacent the channel as provided, for example, in the embodiment depicted in Fig. 12A of the present application. Accordingly, the rejection of Claim 8 should be withdrawn for this additional reason.

Claim 12 recites that "the first planar transistor and the second planar transistor have different threshold voltages." The Office Action states that "different thresholds would have been obvious in view of the difference in function and structure of the two devices." (Office Action at 3). Applicants respectfully submit, however, that Hori does not indicate that the identified first and second planar transistors thereof have different threshold voltages, nor is it clear why the structures would necessarily have different threshold voltages. Accordingly, Applicants respectfully submit that the Office Action fails to make a *prima facie* rejection of Claim 12.

C. The Rejections of Claims 38-40

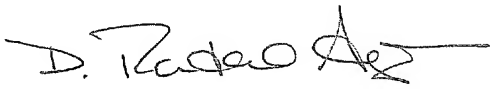
Claims 38-40 stand rejected based on the same combination of references used to reject Claim 1. Applicants respectfully submit that the rejections of Claims 38-40 should

therefore be withdrawn for at least each of the reasons set forth in the discussion of Claim 1 explaining why one of skill in the art would not have been motivated to combine the cited references in the manner suggested. Applicants have also added new Claims 47-57 which depend from Claim 38. Applicants ubmit that each of these new claims is also independently patentable over the cited art.

II. Conclusion

Applicants again wish to thank the Examiner for the thorough examination of the application. Should the Examiner have any questions, please feel free to call Applicants' representative at (919) 854-1422.

Respectfully submitted,



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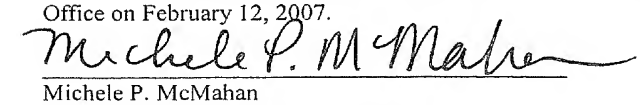

Michele P. McMahan
Date of Signature: February 12, 2007